US007327000B2

(12) **United States Patent**
DeHeer et al.

(10) **Patent No.: US 7,327,000 B2**
(45) **Date of Patent: Feb. 5, 2008**

(54) **PATTERNED THIN FILM GRAPHITE DEVICES AND METHOD FOR MAKING SAME**

(75) Inventors: **Walt A. DeHeer**, Atlanta, GA (US); **Claire Berger**, Atlanta, GA (US); **Phillip N. First**, Doraville, GA (US)

(73) Assignee: **Georgia Tech Research Corp.**, Atlanta, GA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 159 days.

(21) Appl. No.: **11/302,868**

(22) Filed: **Dec. 14, 2005**

(65) **Prior Publication Data**

US 2006/0099750 A1 May 11, 2006

Related U.S. Application Data

(62) Division of application No. 10/860,710, filed on Jun. 3, 2004, now Pat. No. 7,015,142.

(60) Provisional application No. 60/477,997, filed on Jun. 12, 2003.

(51) **Int. Cl.**
H01L 23/62 (2006.01)

(52) **U.S. Cl.** **257/359**; 257/234; 257/E21.041; 257/E21.121; 257/E21.225

(58) **Field of Classification Search** 257/359, 257/226, 228, 234, 382, 414, 427
See application file for complete search history.

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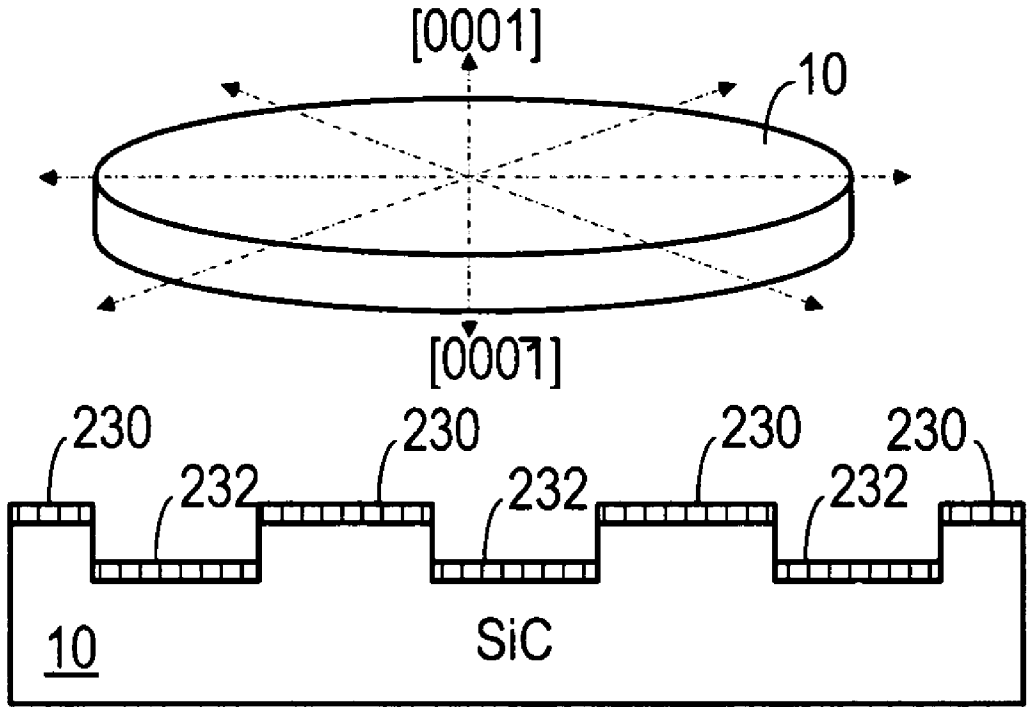
Primary Examiner—David Nhu
(74) *Attorney, Agent, or Firm*—Bryan W. Bockhop; Bockhop & Associates, LLC

(57) **ABSTRACT**

In a method of making graphite devices, a preselected crystal face of a crystal is annealed to create a thin-film graphitic layer disposed against selected face. A preselected pattern is generated on the thin-film graphitic layer. A functional structure includes a crystalline substrate having a preselected crystal face. A thin-film graphitic layer is disposed on the preselected crystal face. The thin-film graphitic layer is patterned so as to define at least one functional structure.

32 Claims, 5 Drawing Sheets



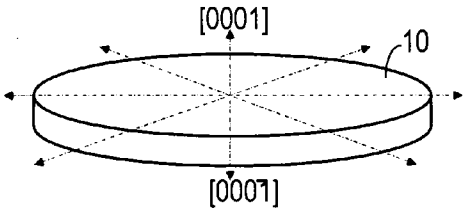


FIG. 1A

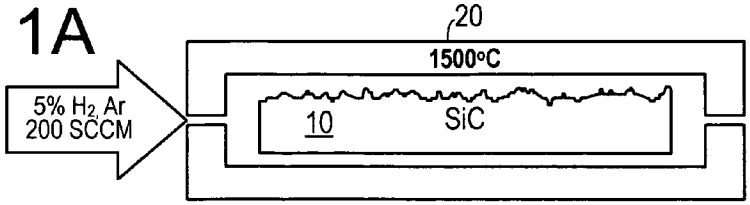


FIG. 1B

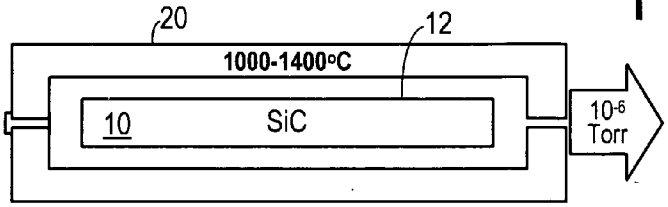


FIG. 1C

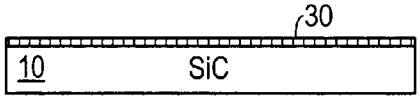


FIG. 1D

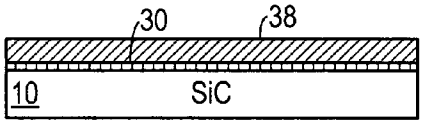


FIG. 1E

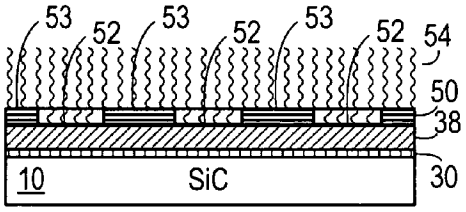


FIG. 1F

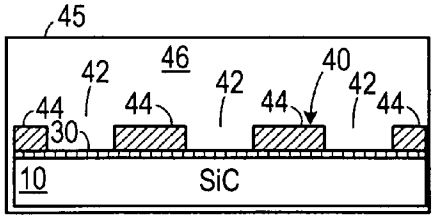


FIG. 1G

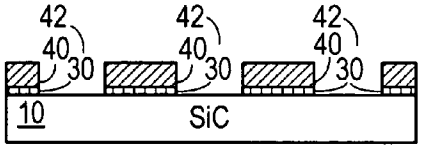


FIG. 1H

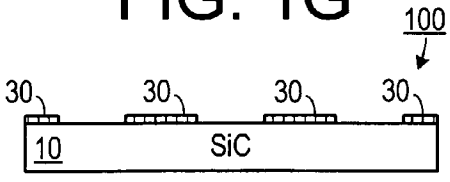


FIG. 1I

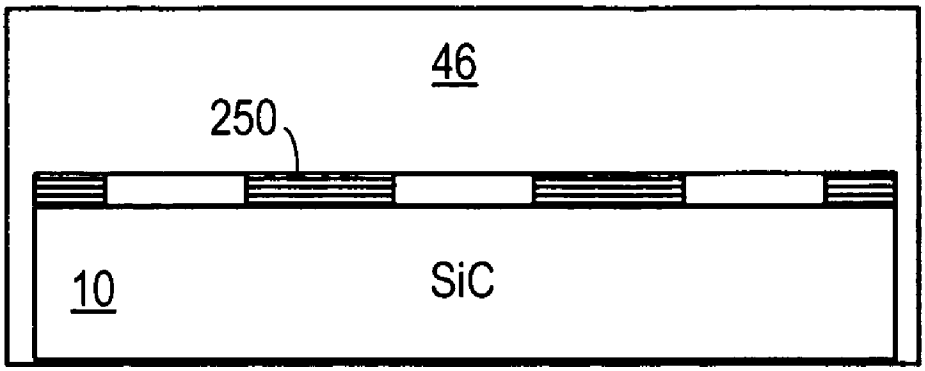


FIG. 2A

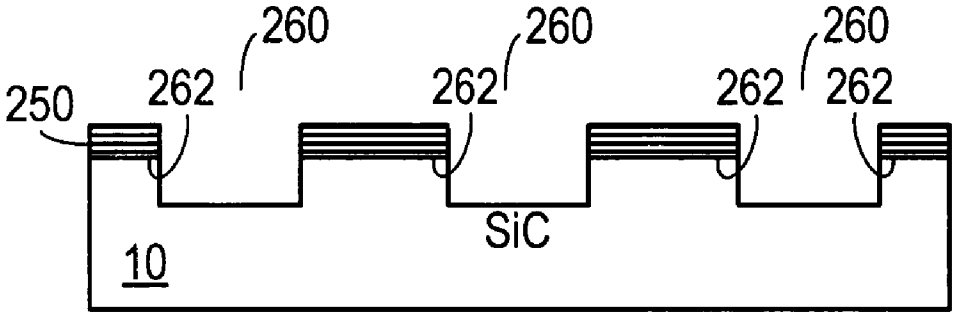


FIG. 2B

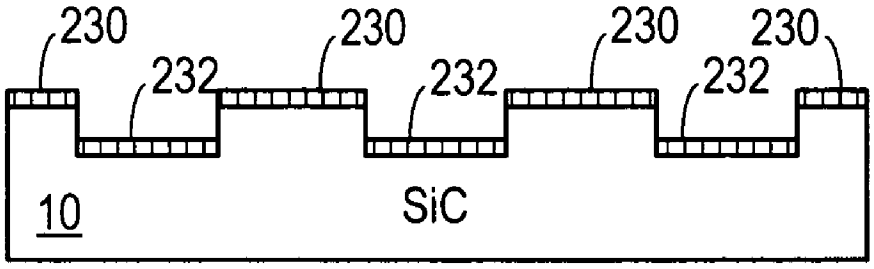


FIG. 2C

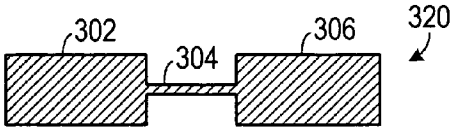


FIG. 3A

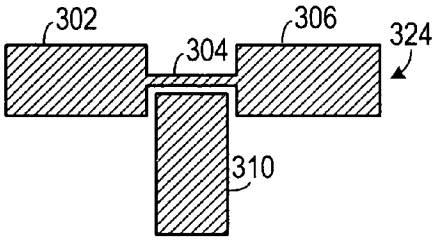


FIG. 3C

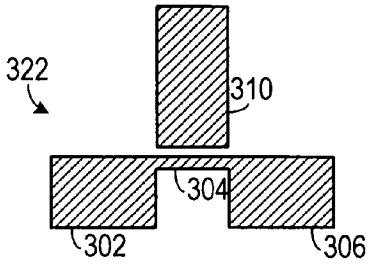


FIG. 3B

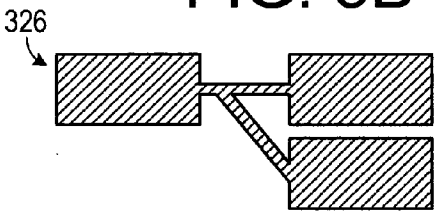


FIG. 3D

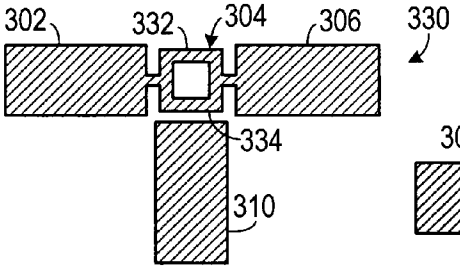


FIG. 3E

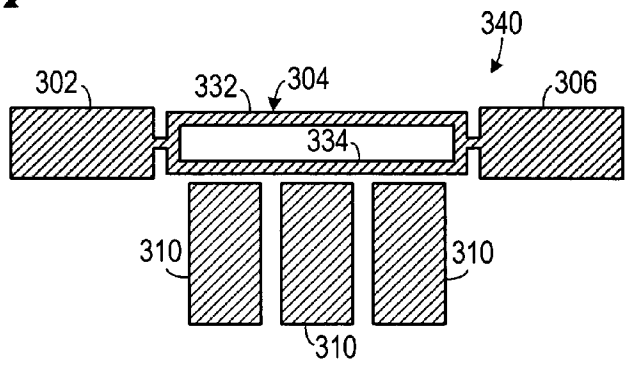


FIG. 3F

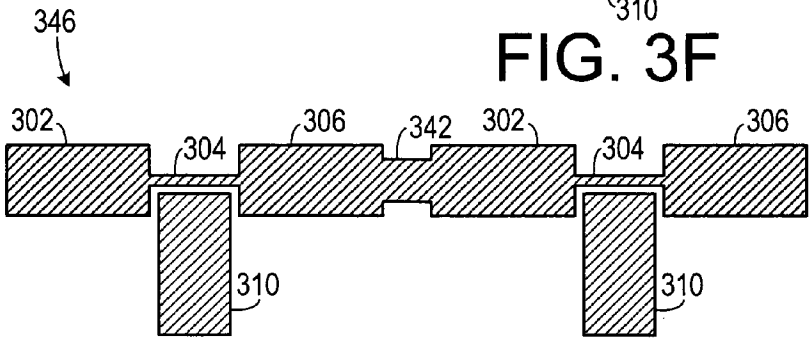


FIG. 3G

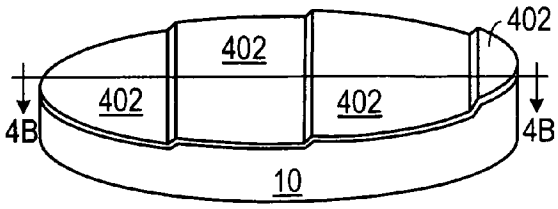


FIG. 4A

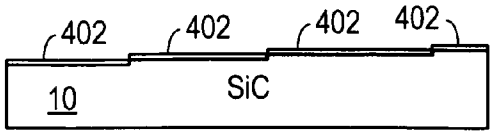


FIG. 4B

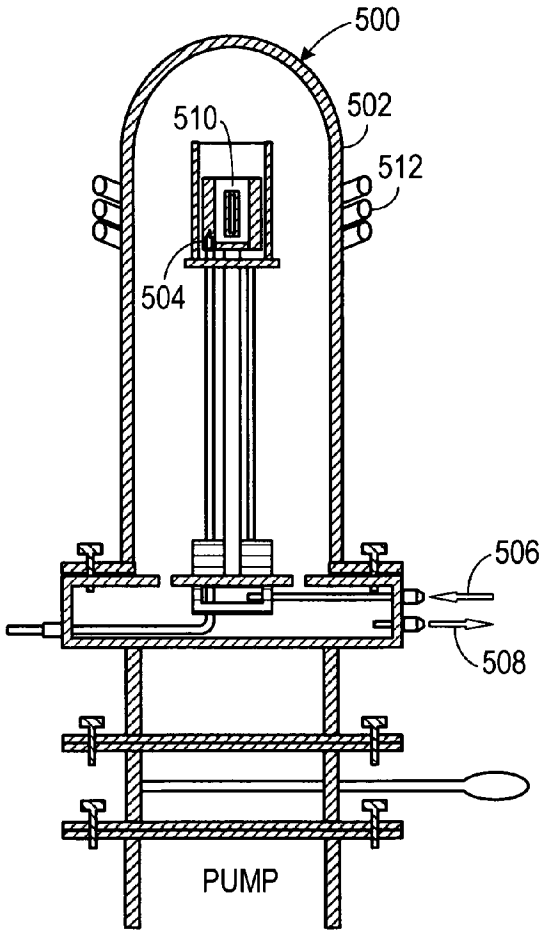


FIG. 5

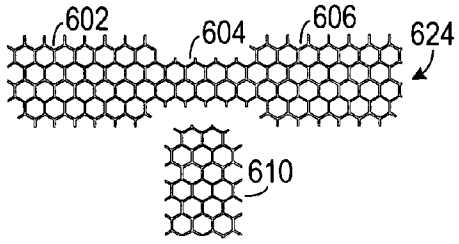


FIG. 6A

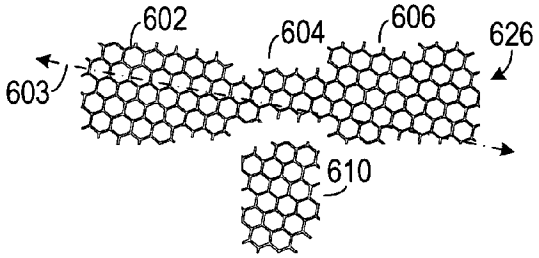


FIG. 6B

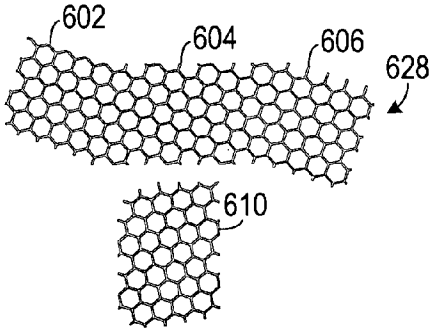


FIG. 6C

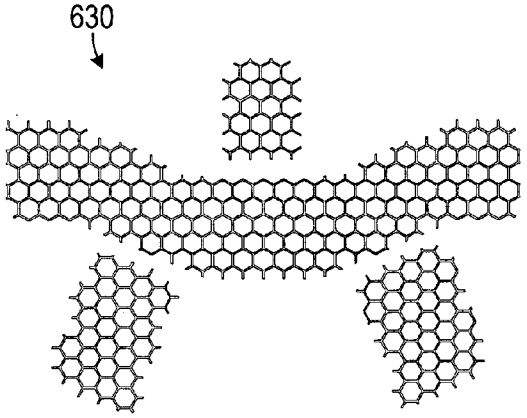


FIG. 6D

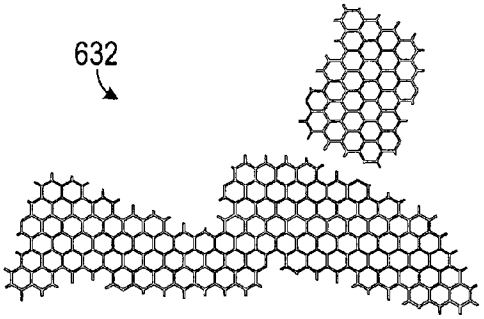


FIG. 6E

PATTERNED THIN FILM GRAPHITE DEVICES AND METHOD FOR MAKING SAME

CROSS-REFERENCE TO A RELATED PATENT APPLICATION

The present application claim is a Divisional application of U.S. patent application Ser. No. 10/860,710, filed on Jun. 3, 2004, U.S. at. No. 7,015,142, entitled "PATTERNED THIN FILM GRAPHITE DEVICES AND METHOD FOR MAKING SAME," the entirety of which is incorporated herein by reference into the disclosure of the present application.

CROSS-REFERENCE TO A PROVISIONAL PATENT APPLICATION

The present application claims priority on U.S. Provisional Patent Application Ser. No. 60/477,997, filed Jun. 12, 2003, entitled "METHOD TO MAKE INTEGRATED AND DISCRETE ELECTRONIC COMPONENTS FROM STRUCTURED THIN GRAPHITIC MATERIALS," the entirety of which is incorporated herein by reference into the disclosure of the present application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to thin film electronic devices and, more specifically, to a system for making thin film graphitic devices.

2. Description of the Prior Art

In modem microelectronics integrated-circuit technology, a silicon wafer is lithographically patterned to accommodate a large number of interconnected electronic components (field effect transistors, resistors, capacitors, etc). The technology relies on the semiconducting properties of silicon and on lithographic patterning methods. Increasing the density of electronic components and reducing the power consumption per component are two of the most important objectives in the microelectronics industry, which has driven the steady reduction in the size of the components in the past decades. However, miniaturization of silicon-based electronics will reach an ultimate limit in the near future, primarily because of limitations imposed by the material properties of silicon, and doped silicon, at the nanoscale.

To sustain the current trend in microelectronics beyond the limits imposed by silicon-based microelectronics technologies, alternative technologies need to be developed. Requirements for such an alternative technology include: smaller feature sizes than feasible with silicon-based microelectronics, more energy-efficient electronics strategies, and production processes that allow large-scale integration, preferably using lithographic patterning methods related to those used in silicon-based microelectronics fabrication.

Several alternatives to silicon-based electronics have been proposed. However, none of the proposed alternatives fulfills all three of the above-listed requirements. For example, molecular electronics is considered to be an attractive alternative to silicon-based electronics. Molecular electronics devices will rely on electronic transport properties through molecules.

One proposed example of molecular electronics employs carbon nanotubes, which are considered to be particularly attractive candidates as building blocks of molecular electronics. Carbon nanotubes are essentially graphite tubes

consisting of one to about 100 graphene layers in tubular configurations. A graphene layer consists of a single layer of carbon atoms arranged in a hexagonal pattern where each atom (except those at the edges) is chemically connected to its three neighbors by sp^2 bonds. Crystalline graphite consists of stacked graphene layers.

The electronic transport properties of carbon nanotubes are due to the π bands of the graphene network. Hence, the electronic properties are directly related to their graphitic structure. Properties of nanotubes include the following: they conduct electrons in either a metallic mode or a semiconducting mode depending on their specific structure; they have been found to be one-dimensional ballistic conductors over micron-scale distances at room temperature; the bandgap of semiconducting nanotubes depends on the diameter of the nanotube, hence it can be tuned depending on its width; they can sustain very large currents (up to 1 mA); they are essentially graphitic and the sp^2 graphite bond ranks among the strongest in nature, making nanotubes exceptionally stable compared to other molecules; and they have been shown to be capable of forming field-effect transistors. Small integrated circuits, involving up to three carbon nanotubes have been demonstrated. These structures consist of several carbon nanotubes that are deposited on an insulating substrate and interconnected with metal wires that are lithographically patterned on top of the nanotubes.

Despite the advantages mentioned above, there are also important disadvantages associated with carbon nanotube-based molecular electronics. For example, since nanotubes are either metallic or semiconducting they must be preselected before they are positioned on the substrate. This aspect by itself currently prohibits large-scale integration of nanotubes. Also, present nanotube configurations are interconnected with metal wires. The Ohmic resistance at each metal-to-nanotube contact is quite large. For example, in the "on" condition, each carbon nanotube transistor exhibits a resistance of several kilo Ohms which means that relatively large amounts of heat are dissipated at the contacts compared with silicon transistors.

Because of these disadvantages, nanotubes are not used yet in commercial integrated electronic circuits. Moreover, integration of carbon nanotube-based electronic devices on a large scale is not expected to be feasible in the foreseeable future.

Therefore, there is a need for an electronic device technology that allows ballistic electron transport at room temperature and that does not exhibit high device interconnect resistance.

SUMMARY OF THE INVENTION

The disadvantages of the prior art are overcome by the present invention which, in one aspect, is a method of making graphite devices in which a preselected face of a substrate is annealed to create a thin-film graphitic layer disposed against preselected face. A preselected pattern is generated on the thin-film graphitic layer.

In another aspect, the invention is a functional structure that includes a crystalline substrate having a preselected crystal face. A thin-film graphitic layer is disposed on the preselected crystal face. The thin-film graphitic layer is patterned so as to define at least one functional structure.

In yet another aspect, the invention is an active electronic device, that includes an electron source area, an electron target area, a substantially flat graphitic strip and a first gate area. The electron target area is spaced apart from the electron source area. The substantially flat graphitic strip is

in electronic communication with the electron source area and the electron target area. The graphitic strip has at least one dimension that includes less than one hundred graphene layers. The first gate area is disposed relative to a first portion of the graphitic strip so that when electronic charge is applied to the first gate area a field is generated that affects an electron transport quality through the first portion of the graphitic strip.

Integrated electronics based on ultra-thin graphite film (UTGF) have several advantages over prior art, these include: large-scale integration is possible using standard microelectronics lithography methods; metals are not used to interconnect the devices so that metal-to-graphite contact resistances are avoided and power dissipation at the contacts is greatly reduced or eliminated; integrated electronic device structures whose operation relies on quantum interference effects can be constructed; feature sizes as small as 1 nm scale are possible and limited only by the lithography methods; and graphite can be electronically modified by chemically bonding molecules to the edges of graphite strips, without damaging the graphitic structure.

These and other aspects of the invention will become apparent from the following description of the preferred embodiments taken in conjunction with the following drawings. As would be obvious to one skilled in the art, many variations and modifications of the invention may be effected without departing from the spirit and scope of the novel concepts of the disclosure.

BRIEF DESCRIPTION OF THE FIGURES OF THE DRAWINGS

FIGS. **1**A-**1**I are schematic diagrams showing a series of process steps according to one illustrative embodiment of the invention.

FIG. **2**A-**2**C are schematic diagrams showing a series of process steps according to a second illustrative embodiment of the invention.

FIG. **3**A-**3**G are plan view schematic diagrams showing a plurality of devices according to one embodiment of the invention.

FIG. **4**A is a top perspective view of a stair-stepped crystal with a graphitic thin film.

FIG. **4**B is a cross-sectional view of the crystal shown in FIG. **4**A, taken along line **4**B-**4**B.

FIG. **5** is a schematic diagram of an experimental apparatus with which may be used for annealing a graphitic film.

FIGS. **6**A-**6**E are schematic diagrams of several exemplary configurations of devices made according to the invention, taking into account crystal lattice orientation.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the invention is now described in detail. Referring to the drawings, like numbers indicate like parts throughout the views. As used in the description herein and throughout the claims, the following terms take the meanings explicitly associated herein, unless the context clearly dictates otherwise: the meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." "Annealing" includes processes in which a substance is heated to a temperature that causes a physical change in the substance, and is not limited to the heating and cooling of metals.

As shown in FIG. **1**A, one method of making a device according to the invention begins with a substrate **10**, such as a crystalline substrate. One example of a crystalline substrate includes silicon carbide. In one embodiment, a 6H crystal of silicon carbide was used and a device according to the invention was produced on the [0001] face of the crystal. As will be appreciated by those of skill in the art, other crystal types (e.g., 3C and 4H, etc.) and other crystal faces may be employed without departing from the scope of the invention.

As shown in FIG. **1**B, the substrate **10** (a cross sectional view is shown in FIG. **1**B) may have an irregular surface that should be flattened. Flattening may be accomplished by exposing the face of the substrate to a reactive gas at a first temperature and first flow pressure for a first amount of time sufficient to remove surface irregularities from the preselected crystal face. For example, a silicon carbide substrate may be placed in a reaction vessel **20** and heated to around 1500° C. with hydrogen gas (in a concentration of about 5% in argon, or some other substantially inert gas) flowing around the substrate **10** at a flow rate of about 200 SCCM for about 20 minutes.

To create a graphitic layer on the flattened surface **12** of the substrate **10**, as shown in FIG. **1**C, the substrate **10** is heated to about 1000° C. to 1400° C. for about 20 minutes at a vacuum of about 10^{-6} Torr. This process may be referred to as "annealing" and it results in the formation of a thin-film graphitic layer **30** on the substrate **10**, as shown in FIG. **1**D. In another illustrative embodiment, the annealing step includes electron beam heating of the substrate **10** at a pressure of substantially 10^{-10} Torr for between 1 minute and 20 minutes. The thin-film graphitic layer **30** could be a graphene layer, which implies only a single layer of carbon atoms forms the layer, or a graphite layer, which implies a plurality of graphene layers. While a minimal number of graphene layers is preferred in some applications, up to 100 graphene layers may be formed without departing from the scope of the invention. (While the vessel **20** is no longer shown for the sake of simplicity, it is readily appreciable that several of the processes employed will take place in some kind of vessel, of a type that would be readily appreciable by those of skill in the chemical arts.)

As shown in FIGS. **1**E-**1**G, a mask **40** is created on the graphitic layer **30** for the purpose of etching (or otherwise removing graphite) a pattern onto the graphitic layer **30**. A photo-resist **38** may be applied to the graphitic layer **30** and a pattern **50** (such as a mask negative) corresponding to a desired functional structure is applied to the photo-resist **38**. The pattern **50** includes a first translucent or transparent region **52** and a second opaque region **53**. The pattern **50** is exposed to a predetermined electromagnetic energy **54**, thereby causing structural change in exposed portions of the photo-resist **38**. The photo-resist **38** is then developed so as to remove undesired portions of the photo-resist **38**, thereby creating the mask **40** that corresponds to a desired functional structure (such as a transistor).

The mask **40** includes at least one non-masking region **42** in which a portion of the thin-film graphitic layer **30** is exposed to an environment **45** and at least one masking region **44** in which a second portion of the thin-film graphitic layer **30** is not exposed to an environment **45**. A reactive substance **46** is released into the environment **45**. The reactive substance **46** could be one of many substances that are reactive with graphite. For example, an ionic plasma, such as an oxygen plasma, may be employed as a reactive substance **46**. The reactive substance **46** removes graphite from the thin-film graphitic layer **30** so as to form a functional structure **100** in the thin-film graphitic layer **32**, as shown in FIGS. **1**H and **1**I.

As shown in FIGS. **2**A-**2**C, in an alternate embodiment, the mask **250** is applied directly to the crystal face of the substrate **10** prior to any annealing. The reactive substance **46** creates voids **260** in the substrate **10** and leaves plateaus **262** in areas covered by the mask **260**. The mask **250** may be removed and the substrate **10** may be annealed to generate a high level graphitic layer **230** and a low level graphitic layer **232**, both of which may be used if a suitable geometry is chosen.

As shown in FIG. **3**A, a simple functional structure **320**, such as an electronic device, made according to the invention, can be made by patterning the graphitic layer to have an electron source area **302** and an electron target, or drain, area **306** that are interconnected via a graphitic strip **304**, which could be a graphene strip or a nano-scale graphite strip. The edges or the surface, or both, of the graphitic strip **304** may be functionalized with a dopant so that electron transport through the graphitic strip **304** may be affected by interaction between the dopant and the environment to which the graphitic strip **304** is exposed.

As shown in FIGS. **3**B and **3**C, a transistor may be made by disposing a gate area **310** adjacent to the graphitic strip **304** so that an electron transport property of the graphitic strip **304** changes when charge is applied to the gate portion so as to induce a field that interacts with the graphitic strip **304**. A transistor can take the form shown as transistor **322** or transistor **324**. A directional coupler **326** configuration is shown in FIG. **3**D. The field may be, for example, an electric field or a magnetic field. As used herein, "gate" includes anything that generates field, whether magnetic or electrical, that can affect electron transport through a graphitic strip. It should be noted that Schottky-type gating is possible, in which case the gate electrode may be seamlessly connected to the graphitic strip.

An interferometer configuration **330**, such as a Mach-Zender interferometric device, is show in FIG. **3**E. The interferometer configuration **330** includes a loop-like structure **304** that has a first branch **334** and a spaced-apart second branch **332** in electrical communication with the source member **302** and with the drain member **306**. A gate member **310** is disposed adjacent to the first branch **334** so that it is capable of exerting an electrical field substantially only on the first branch **334**. The interference may be sensed by a change in the source-to-drain current. Alternately, a sensor (not shown), such as a "beat" counter can be used to sense interference between electrons passing through the first branch **334** and electrons passing through the second branch **332**. In this embodiment, a selected one of the first branch **334** or the second branch **332** may be doped with a functionalizing dopant. A multi-gate interferometric device **340**, as shown in FIG. **3**F, could be used to generate logic functions. One advantage of the invention is that compound devices, such as device **346** shown in FIG. **3**G, may be formed entirely out of the graphitic layer, with inter-device connections **342** being formed from the graphitic layer. This would allow the formation of virtually all logic gates and electronic components used in computers and other electronic devices. Devices of the type shown could employ gates that are coplanar with the graphitic strips, or the gates could be in a stacked relationship if an insulator is applied between the graphitic strip and the gate.

These devices could include reactive molecules attached to the graphitic strips, either at the edges or on the surfaces, where the reactive molecules are capable of reacting to a target substance. Thus, if the target substance is present in an environment to which the graphitic strip is exposed, a change in current flow through the graphitic strip will occur as a result of the exposure. This configuration could find substantial utility in environmental sensor applications.

As shown in FIGS. **4**A and **4**B, the substrate crystal **10** may not be perfectly flat, but may have a stair-stepped surface **402** after flattening.

One exemplary experimental apparatus **500** for making devices according to the invention includes a reaction vessel **502**, a sample space **510** into which is placed the substrate, a gas intake **506** and a gas outlet **508**. A heating element **512** applies heat to the vessel **502** and a thermocouple **504** may be employed to control temperature of the sample space **510**. As will be appreciated by those of skill in the art, many other types of apparatus may be employed to make structures according to the invention.

With the invention, a continuous ultrathin graphite film (UTGF) on an insulating substrate is patterned, to produce an interconnected electronic device (i.e. integrated electronic circuit). The electronic structure of a strip of UTGF is related to that of a carbon nanotubes of similar dimensions, and it has properties that are similar to those of carbon nanotubes. For example, a narrow graphene strip (with a width from 1 to 100 nm) is a one dimensional conductor, is either metallic or semiconducting depending on its structure, and the band gap for a semiconducting graphene strip is inversely proportional to its width. It is expected that narrow graphene strips will be room temperature ballistic conductors on size scales of at least 100 nm.

The invention disclosed here has several advantages compared with nanotube-based electronics yet it retains the essential advantages of nanotube-based electronics. In particular, the invention allows production of integrated circuits of planar graphite devices. An important feature of the integrated structures is that the active elements (transistors, for example) and their interconnects are fashioned from a single graphite layer by patterning the graphite layer. In this way, the devices and the leads to the devices may be of the same graphitic material (i.e. UTFG) and they may be seamlessly connected to each other. This arrangement significantly reduces power dissipation at the lead-device contacts. Another advantage is that integrated circuits can be patterned using standard lithography techniques.

It should be noted that the inventors have experimentally demonstrated that ultra-thin graphite films produced on silicon carbide can be gated using the field effect. It is currently believed that thick graphite films cannot be gated.

As shown in FIGS. **6**A-**6**E, crystal orientation could affect electron transport from an electron source **602** to an electron target **606** through the graphitic strip **604**, with a gate **610** affecting electron transport. It should be noted that FIGS. **6**A-**6**E are schematic diagrams intending to give the impression of graphitic carbon rings in the devices shown and are not drawn to scale. Most graphitic devices would include many more carbon rings than shown. However, the lesser number of rings is shown for the sake of simplifying the image of the device. A device **624** taken along a linear orientation of carbon unit cells in shown in FIG. **6**A. Orientation along another axis **603** may be chosen, as shown in FIG. **6**B, which would render different electron transport properties for a device **626**. More complex devices **628** and **630**, as shown in FIG. **6**C and FIG. **6**D, respectively, may take advantage of electron transport properties that change as crystal orientation changes. An irregular geometry may be chosen for the device **632**, as shown in FIG. **6**L, to take advantage of the electron transport property of such a configuration.

While not shown explicitly herein, graphitic structures typically have "hanging bonds" where a carbon atom is not

bonded to at least three other carbon atoms, as is typical at the edge of a structure. Such hanging bonds are reactive and can be passivated by exposing them to hydrogen or functionalized by exposing them to a dopant. An advantage of functionalizing is that it could change the Fermi level in the structure so as to render a desired property in the structure.

The above described embodiments are given as illustrative examples only. It will be readily appreciated that many deviations may be made from the specific embodiments disclosed in this specification without departing from the invention. Accordingly, the scope of the invention is to be determined by the claims below rather than being limited to the specifically described embodiments above.

What is claimed is:

1. A functional structure, comprising:

a. a crystalline substrate having a preselected crystal face; and

b. a thin-film graphitic layer disposed on the preselected crystal face, the thin-film graphitic layer patterned so as to define at least one functional structure.

2. The functional structure of claim **1**, wherein the crystalline substrate comprises silicon carbide.

3. The functional structure of claim **1**, wherein the substrate comprises an insulator.

4. The functional structure of claim **1**, wherein the thin-film graphitic layer has a nano-scale thickness.

5. The functional structure of claim **1**, wherein the thin-film graphitic layer comprises a graphene strip.

6. The functional structure of claim **5**, wherein the graphene strip includes an edge that is functionalized with a dopant.

7. The functional structure of claim **1**, wherein the thin-film graphitic layer comprises a graphite strip.

8. The functional structure of claim **5**, wherein the graphite strip includes an edge that is functionalized with a dopant.

9. The functional structure of claim **1**, wherein the thin-film graphitic layer is patterned to form an electronic device.

10. The functional structure of claim **5**, wherein the electronic device comprises a transistor.

11. The functional structure of claim **10**, wherein the transistor comprises:

a. a graphite source member;

b. a graphite drain member, spaced apart from the graphite source member;

c. a graphite connector, in electrical communication with both the graphite source member and the graphite drain member; and

d. a gate portion spaced apart from the graphite connector at a distance such that an electron transport property of the graphite connector changes when charge is applied to the gate portion so as to induce a field that interacts with the graphite connector.

12. The functional structure of claim **5**, wherein the electronic device comprises a logic gate.

13. The functional structure of claim **5**, wherein the electronic device comprises a logic directional coupler.

14. The functional structure of claim **5**, wherein the electronic device comprises an interferometer.

15. The functional structure of claim **14**, wherein the interferometer comprises:

a. a source member;

b. a drain member;

c. a loop-like structure, having a first branch and a spaced-apart second branch, in electrical communication with the source member and with the drain member;

d. at least one gate member disposed adjacent to the first branch, that is capable of exerting an electrical field substantially only on the first branch; and

e. a sensor that is configured to sense interference between electrons passing through the first branch and electrons passing through the spaced-apart second branch.

16. The functional structure of claim **15**, wherein a portion of a selected one of the first branch and the spaced-apart second branch comprises a functionalizing dopant.

17. The functional structure of claim **14**, wherein the interferometer comprises a Mach-Zender device.

18. An active electronic device, comprising:

a. a first electron source area;

b. a first electron target area, spaced apart from the first electron source area;

c. a substantially flat graphitic strip that is in electronic communication with the first electron source area and the electron first target area, the flat graphitic strip having at least one dimension that includes less than one hundred graphene layers;

d. a first gate area, disposed relative to a first portion of the flat graphitic strip so that when electronic charge is applied to the first gate area, a field is generated that affects an electron transport quality through the first portion of the flat graphitic strip.

19. The active electronic device of claim **18**, wherein the graphitic strip has a plurality of preselected molecules attached thereto, the preselected molecules capable of reacting to a target substance so that when the target substance is present in an environment and when the graphitic strip is exposed to the environment then a change in current flow through the graphitic strip will occur.

20. The active electronic device of claim **18**, wherein the graphitic strip comprises a single graphene layer.

21. The active electronic device of claim **18**, wherein the first gate area and the graphitic strip are substantially coplanar.

22. The active electronic device of claim **18**, wherein the first gate area and the graphitic strip are in a substantially stacked relationship.

23. The active electronic device of claim **18**, wherein the field is an electric field.

24. The active electronic device of claim **18**, wherein the field is a magnetic field.

25. The active electronic device of claim **18**, wherein the graphitic strip comprises a loop portion that includes a first branch and a second branch, the second branch diverting from the first branch at a first location and rejoining the first branch at a second location, spaced apart from the first location, the gate area disposed relative to the first branch and the second branch so that a field generated at the gate area affects the electron transport quality through the first branch in a first manner and in the second branch in a second manner, different from the first manner.

26. The active electronic device of claim **25**, further comprising at least one second gate area, spaced apart from the first gate area, and disposed relative to a second portion of the graphitic strip so that when electronic charge is applied to the second gate area, a field is generated that affects an electron transport quality through the second portion of the graphitic strip.

27. The active electronic device of claim **26**, wherein the first portion and the second portion are both disposed on the first branch.

28. The active electronic device of claim **26**, wherein the first portion is disposed on the first branch and the second portion is disposed on the second branch.

29. The active electronic device of claim 25, wherein a selected one of the first branch and the second branch is functionalized so that the active electronic device functions as an interferometric sensor.

30. The active electronic device of claim 25, wherein a magnetic field affects the electron transport quality.

31. The active electronic device of claim 18, wherein the first electron source area and the first electron target area each include a graphitic surface, the active electronic device further comprising:

a. a second electron source area including a graphitic surface; and

b. a second electron target area including a graphitic surface,

wherein a selected one of the first electron source area and the first electron target area is electrically coupled to a selected one of the second electron source area and the second electron target area via a graphitic surface.

32. The active electronic device of claim 18, wherein the first electron source area and the first electron target area each include a graphitic surface, the active electronic device further comprising:

a. a second electron source area including a graphitic surface;

b. a second electron target area including a graphitic surface; and

c. a second gate area including a graphitic surface,

wherein selected ones of the fist electron source area, the first target area, and the first gate area are electrically coupled to selected ones of the second electron source area, the second target area, and the second gate area via a graphitic surface.

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